This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (original): A semiconductor memory comprising:

a memory cell comprising at least one first MOS transistor having a threshold level of at or near 0V and at least one capacitor to store information electrically connected to an electrode of said first MOS transistor;

a word line electrically connected to a gate of said first MOS transistor;

a bit line electrically connected to the first MOS transistor at a node of said first transistor different from the electrode of said first MOS transistor where the capacitor is connected; and

a sense amplifier which compares voltage on the bit line with a reference voltage and amplifies the voltage difference.

2 (original): The semiconductor memory according to claim 1, wherein the capacitor employs a ferroelectric thin film as an insulator between the electrodes thereof.

3 (original): The semiconductor memory according to claim 1, wherein the capacitor employs a gate oxide film as an insulator between the electrodes thereof.

4 (original): The semiconductor memory according to claims 1, wherein a voltage to which the word line is electrically elevated is equal to a supply voltage.

5 (original): The semiconductor memory according to claims 2, wherein a voltage to which the word line is electrically elevated is equal to a supply voltage.

6 (original): The semiconductor memory according to claims 3, wherein a voltage to which the word line is electrically elevated is equal to a supply voltage.

7 (original): The semiconductor memory according to claim 1, wherein a voltage on the word line is a negative value when the word line is not selected.

8 (original): The semiconductor memory according to claim 5, wherein a voltage on the word line is a negative value when the word line is not selected.

9 (original): The semiconductor memory according to claim 6, wherein a voltage on the word line is a negative value when the word line is not selected.

10 (original): The semiconductor memory according to claim 4, wherein a voltage on the word line is a negative value when the word line is not selected.

11 (original): The semiconductor memory according to claim 1, wherein a voltage on a lower voltage side of the sense amplifier is a positive value.

12 (original): The semiconductor memory according to claim 2, wherein the voltage on a lower voltage side of the sense amplifier is a positive value.

13 (original): The semiconductor memory according to claim 3, wherein the voltage on a lower voltage side of the sense amplifier is a positive value.

14 (original): The semiconductor memory according to claim 4, wherein the voltage on a lower voltage side of the sense amplifier is a positive value.

15 (original): The semiconductor memory according to claim 5, wherein the voltage on a lower voltage side of the sense amplifier is a positive value.

16 (original): The semiconductor memory according to claim 6, wherein the voltage on a lower voltage side of the sense amplifier is a positive value.

17 (original): A semiconductor memory comprising:

a memory cell unit comprising a plurality of memory cells in each of which electrodes of a ferroelectric capacitor are electrically connected to a source and a drain of a first MOS transistor, respectively;

a plurality of word lines each of which is electrically connected to a gate of said first MOS transistor;

a plate line electrically connected to one of the two electrodes of said memory cell unit;

a switch which is used to select a block and which is electrically connected to the other one of the two electrodes of the memory cell unit;

a bit line electrically connected to the first MOS transistor; and

a sense amplifier to compare and amplify voltages of a bit line pair of the bit line and its complementary bit line;

wherein the first MOS transistor has a threshold level of at or near 0V.

18 (original): The semiconductor memory according to claim 17, wherein a voltage to which the word line is electrically elevated is equal to a supply voltage.

19 (original): The semiconductor memory according to claim 17, wherein the voltage on the word line is a negative value when the word line is not selected.

20 (original): The semiconductor memory according to claim 18, wherein the voltage on the word line is a negative value when the word line is not selected.

21 (original): The semiconductor memory according to claim 17, wherein the voltage on the lower voltage side of the sense amplifier is a positive value.

22 (original): A ferroelectric memory comprising:

a memory cell unit comprising a plurality of memory cells in each of which one of the two electrodes of a ferroelectric capacitor is electrically connected to a source of a first MOS transistor and the other one of the two electrodes is electrically connected to the drain thereof;

a plurality of word lines each of which is electrically connected to a gate of said first MOS transistor;

a plate line electrically connected to one of the two electrodes of said memory cell unit;

a bit line electrically connected to the other one of the two electrodes of the memory cell unit via a block select switching device;

a sense amplifier to compare and amplify voltages of a bit line pair of said bit line and its complementary bit line;

a pair of second transistors each of which receives the voltage of the bit line pair at each control electrode, the pair of input/output nodes of the sense amplifier being electrically connected between each pair of the electrodes of the second transistors; and

a pair of third transistors for data writing each of which is inserted between the pair of the input/output nodes of the sense amplifier and the bit line pair, and controlled to convey data which was amplified by the sense amplifier to the bit line pair.

23 (original): The ferroelectric memory according to claim 22, further comprising an equalization circuit connected between the bit line pair, for equalizing the bit line pair to 0V with a specific timing.

24 (original): A ferroelectric memory comprising:

a memory cell array comprising a plurality of memory cells in each of which an electrode of a first MOS transistor is electrically connected to an electrode of at least one ferroelectric capacitor;

a word line which is electrically connected to a gate of said first MOS transistor;

a bit line electrically connected to the first transistor at a node of said first transistor different from the electrode of said first MOS transistor where the ferroelectric capacitor is electrically connected;

a plate line electrically connected to the ferroelectric capacitor at a node of said capacitor different from the electrode of said capacitor where the first MOS transistor is electrically connected;

a sense amplifier to compare and amplify voltages of a bit line pair of said bit line and its complementary bit line;

an equalization circuit connected between the bit line pair, for equalizing the bit line pair to 0V with a specific timing; and

a second MOS transistor inserted between the equalization circuit and the sense amplifier, for selectively disconnecting the equalization circuit and the sense amplifier from each other, with a disconnection control signal applied to a gate thereof.

25 (currently amended): A semiconductor memory comprising:

a memory cell comprising at least one ~~first~~ MOS transistor having a threshold level of at or near 0V and at least one capacitor to store information electrically connected at one terminal thereof to ~~an electrode~~ one of source/drain electrodes of ~~said first~~ the MOS transistor;

a word line electrically connected to a gate of ~~said first~~ the MOS transistor;

a bit line electrically connected to the other of source/drain electrodes of the ~~first~~ MOS transistor ~~at a node of said first MOS transistor different from the electrode of said first MOS transistor where the capacitor is connected~~;

a plate line connected to the other terminal of the capacitor; and

a sense amplifier which compares voltages on the bit line and ~~its~~ a complementary bit line and amplifies the voltage difference.

26 (original): A ferroelectric memory comprising:

a memory cell unit comprising a plurality of memory cells in each of which one of the two electrodes of a ferroelectric capacitor is electrically connected to a source of a first MOS transistor having a threshold level of at or near 0V and the other electrode to a drain thereof;

a plurality of word lines each of which is electrically connected to a gate of said first MOS transistor;

a plate line electrically connected to one of the two electrodes of said memory cell unit;

a bit line electrically connected to the other of the two electrodes of the memory cell unit via a block select switching device;

a sense amplifier to compare and amplify voltages of a bit line pair of said bit line and its complementary bit line; and

an equalization circuit connected between the bit line pair, for equalizing the bit line pair to 0V with a specific timing.

27 (original): A semiconductor memory comprising:

a memory cell comprising at least one first MOS transistor having a threshold level of at or near 0V and at least one capacitor to store information electrically connected at one terminal thereof to an electrode of said first MOS transistor, the other terminal of the capacitor being connected to a predetermined power supply potential;

a word line electrically connected to a gate of said first MOS transistor;

a bit line electrically connected to the first MOS transistor at a node of said first MOS transistor different from the electrode of said first MOS transistor where the capacitor is connected; and

a sense amplifier which compares voltages on the bit line and its complementary bit line and amplifies the voltage difference.

28 (new): A semiconductor memory according to claim 25, wherein a voltage of the word line is raised to a power supply voltage VCC.

29 (new): A semiconductor memory according to claim 25, wherein an equalization voltage for the bit lines is controlled to be a value higher than 0V.

30 (new): A semiconductor memory comprising:

a memory cell including at least one intrinsic type MOS transistor and at least one capacitor to store information electrically connected at one terminal thereof to one of source/drain electrodes of the MOS transistor;

a word line electrically connected to a gate of the MOS transistor;

a bit line electrically connected to the other of source/drain electrodes of the MOS transistor;

a plate line connected to the other terminal of the capacitor; and

a sense amplifier which compares the voltages on the bit line and a complementary bit line and amplifies the voltage difference.

31 (new): A semiconductor memory according to claim 30, wherein a voltage of the word line is raised to a power supply voltage VCC.

32 (new): A semiconductor memory according to claim 30, wherein an equalization voltage for a pair of the bit lines is controlled to be a value higher than 0V.